1. A memory cell comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.

2. The memory cell of claim 1, wherein the source comprises a buried layer.

3. The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate.

4. The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate defined by a spacer.

5. The memory cell of claim 1, wherein the horizontal floating gate comprises a self aligned floating gate.

6. A memory cell having a square feature size of less than $4F^2$ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel;

a substantially horizontal floating gate formed over at least a portion of the drain; and

a substantially vertical select gate formed substantially perpendicular to the horizontal floating gate in a trench, wherein the select gate is adjacent to the vertical channel.

7. The memory cell of claim 6, wherein the memory cell has a minimum feature size corresponding to the horizontal floating gate and the vertical select gate.

8. The memory cell of claim 6 further comprising a select source and a select drain coupled to the select gate, wherein the select source, the s lect gate and the select drain form a select transistor.

9. The memory cell of claim 6, wherein the memory cell has a square feature size not greater than $2F^2$.

10. (Amended) A memory cell having a square feature size of less than $4.5F^2$ comprising:

a first transistor comprising a source, a drain and a gate, wherein the source and drain are arranged substantially vertically and the gate is horizontally positioned such that at least a portion of the gate overlies at least a portion of the drain; and

a select transistor coupled to the first transistor, comprising a source, a drain and a gate, wherein the gate of the select transistor is formed substantially vertically and perpendicular to the gate of the first transistor relative to a vertical plane.

11. The memory cell of claim 10, wherein the drain of the first transistor has an upper surface and a lower surface and the source of the first transistor has an upper surface and a lower surface and the upper surface of the source of the first transistor is located below the lower surface the drain of the first transistor.

12. The memory cell of claim 10, wherein the source and drain of the first transistor are shared as the source and drain of the select transistor.

13. (Canceled)

14. (Canceled)

15. A memory device having a square feature size of less than $4F^2$ comprising:

a horizontal first n-type layer formed over a substrate;

a p-type layer formed over the first n-type layer;

a horizontal second n-type layer formed over the p-type layer;

a horizontal floating gate formed over the substrate; and

a vertical select gate formed over the substrate, wherein the p-type layer forms a vertical channel, the first n-type layer forms a buried source and the second n-type layer forms a drain.

16. The memory device of claim 15, wherein the vertical select gate is formed substantially perpendicular to the horizontal floating gate.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate;

a p-type layer formed over the first n-type layer;

a second n-type layer formed over the p-type layer;

a floating gate formed over the substrate;

a trench formed in the p-type layer; and

a select gate formed on a sidewall of the trench.

21. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate forming a source;

a p-type layer formed over the first n-type layer forming a vertical channel;

a second n-type layer formed over the p-typ layer forming a drain;

a tunnel oxide layer formed over at least a portion of the second n-type layer;

a first poly layer formed over at least a portion of the tunnel oxide layer;

trenches formed in the p-type layer; and

a select gate formed on sidewalls of the trenches.

22. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer, said substrate comprising:;

a buried source formed in the substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel;

a tunnel oxide layer formed over at least a portion of the drain;

a floating gate formed over the tunnel oxide layer such that at least a portion of the floating gate overlies at least a portion of the drain;

a select trench formed in the substrate;

a select gate formed along sidewalls of the select trench;

an active trench formed generally over the drain; and

a conductive layer formed in the active trench.

23. (Twice Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the p-type layer;

a vertical select gate formed in the select trench;

digitlines formed over, and capable of electrical communication with the second n-type layer;

a floating gate formed over the p-type layer such that at least a portion of the floating gate overlies at least a portion of the second n-type layer; and

wordlines formed over the substrate and the digitlines.

24. A memory device having a square feature size of less than $4F^2$ comprising:
a first n-type layer formed over a substrate;
a p-type layer formed over the n-type layer;
a second n-type layer formed in the p-type layer;
a select trench formed in the substrate;
a vertical select gate formed in the select trench;
a conductive layer formed over at least a portion of the second n-type layer;
a first spacer formed on the conductive layer;
a tunnel oxide layer formed over at least a portion of the substrate;
a polysilicon layer formed on the tunnel oxide layer; and
an oxide layer formed on the polysilicon layer.

25. The memory device of claim 24, wherein the conductive layer comprises a tungsten layer.

26. (Twice Amended) A memory device comprising:
a first n-type layer formed over a substrate defining a source;
a p-type layer formed over the n-type layer;
a second n-type layer formed in the p-type layer defining a drain;
a select trench formed in the p-type layer;
a select gate formed substantially vertical in the select trench; and
a floating gate formed over the p-type layer so as to avoid the select trench.

27. The memory device of claim 26, further comprising a tunnel oxide layer formed over the substrate.

28. The memory device of claim 27, further comprising digitlines and wordlines formed over the substrate.

29. Th memory device of claim 28, wherein the wordlines are above the digitlines.

30. The memory device of claim 29, wherein the wordlines comprise a poly-WSi layer.

31. The memory device of claim 30, wherein the digitlines comprise at least one tungsten layer.

32. The memory device of claim 31, wherein the digitlines are above at least a portion of the drain.

33. The memory device of claim 32 further comprising a spacer formed between the digitlines and the wordlines.

34. The memory device of claim 26, wherein the drain is doped with Boron.

35. The memory device of claim 26, wherein the floating gate comprises tunnel oxide, polysilicon and oxide layers.

36. The memory device of claim 26, wherein the floating gate is self aligned.

Please add the following new claims:

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69. (New) A memory device comprising:

a substrate;

a buried source formed in the substrate;

a first layer formed over the substrate;

a first drain formed in the first layer generally over the buried source defining a first substantially vertical channel therebetween;

a trench formed in the first layer;

a select gate formed in the trench; and

a first floating gate formed over the first layer adjacent to the trench and proximate to the first substantially vertical channel.

70. (New) The memory device according to claim 69, further comprising

a second drain formed in the first layer generally over the buried source defining a second substantially vertical channel therebetween; and

a second floating gate formed over the first layer adjacent to the trench and proximate to the second substantially vertical channel, wherein the

71. (New) The memory device according to claim 69, wherein the floating gate defines a horizontal floating gate arranged over the first layer such that at least a portion of the floating gate overlies at least a portion of the drain.

72. (New) The memory device according to claim 69, wherein the floating gate defines a horizontal floating gate further arranged generally above the substantially vertical channel.

73. (New) The memory device according to claim 69, wherein the trench extends through the first layer to the buried source.

74. (New) A memory device comprising:

a first layer defining a source;

a second layer formed over the first layer;

a drain formed in the second layer generally over the source defining a substantially vertical channel therebetween;

a trench formed in the second layer;

a select gate formed in the trench; and

a floating gate formed over the second layer adjacent to the trench.

75. (New) The memory device according to claim 74, wherein the floating gate defines a horizontal floating gate arranged over the second layer such that at least a portion of the floating gate overlies at least a portion of the drain.

76. (New) The memory device according to claim 74, wherein the trench extends through the second layer and into the first layer.

77. (New) The memory device according to claim 74, wherein the floating gate defines a horizontal floating gate further arranged generally above the substantially vertical channel.